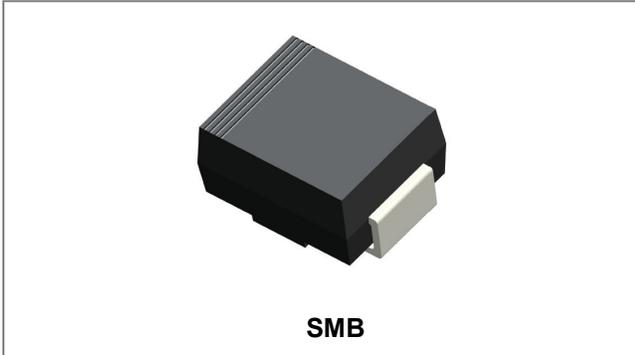


ER3GB ULTRAFAST RECTIFIER



Features

- Glass Passivated Die Construction
- Ideally Suited for Automatic Assembly
- Low Forward Overload Drop, High Efficiency
- Low Power Loss
- Super-Fast Recovery Time
- Plastic Case Material has UL Flammability Classification Rating 94V-0
- This is a Pb – Free Device
- All SMC parts are traceable to the wafer lot
- Additional testing can be offered upon request

Circuit Diagram



Mechanical Data

- Case: Low Profile Molded Plastic
- Terminals: Solder Plated, Solderable per MIL-STD-750, Method 2026
- Polarity: Cathode Band or Cathode Notch
- Marking: Type Number
- Weight: 0.09grams(approx)

Maximum Ratings and Electrical Characteristics @T_A=25°C unless otherwise specified

Characteristic	Symbol	ER3GB	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V _{RRM} V _{RWM} V _R	400	V
Average Rectified Output Current @T _L = 75°C	I _o	3.0	A
Non-Repetitive Peak Forward Surge Current 8.3ms Single half sine-wave superimposed on rated load (JEDEC Method)	I _{FSM}	100	A
Forward Voltage @I _F = 3.0A, T _J =25°C	V _F	1.25	V
Peak Reverse Current @T _A = 25°C At Rated DC Blocking Voltage @T _A = 100°C	I _{RM}	5.0 500	μA
Typical Thermal Resistance Junction to Lead (Note 1)	R _{θJL}	16	K/W
Maximum Reverse Recovery Time (Note 2)	T _{rr}	35	ns
Typical Junction Capacitance (Note 3)	C _J	45	pF
Operating and Storage Temperature Range	T _J , T _{STG}	-65 to +150	°C

Note: 1. Mounted on P.C. Board with 8.0mm² lead area
 2. Measured with I_F=0.5A, I_R=1.0A, I_{rr}=0.25A,
 3. Measured at 1.0 MHZ and applied reverse voltage of 4.0 V_{DC}

Ratings and Characteristics Curves

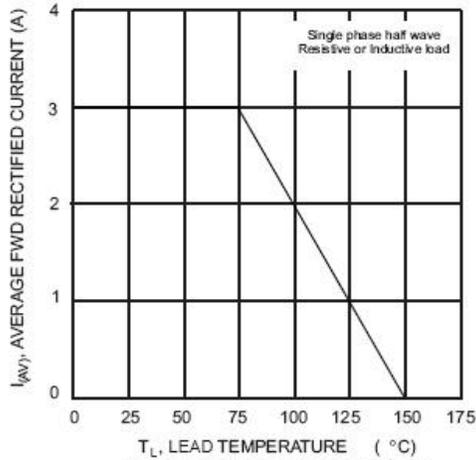


Fig. 1 Forward Current Derating Curve

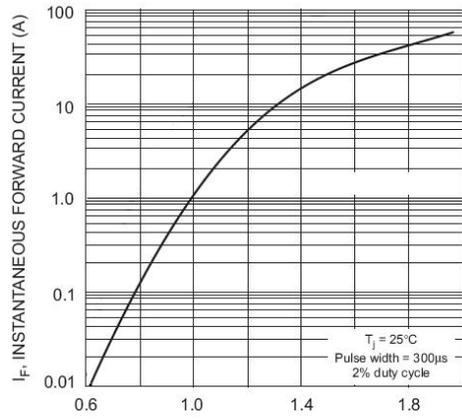


Fig. 2 Typical Forward Characteristics

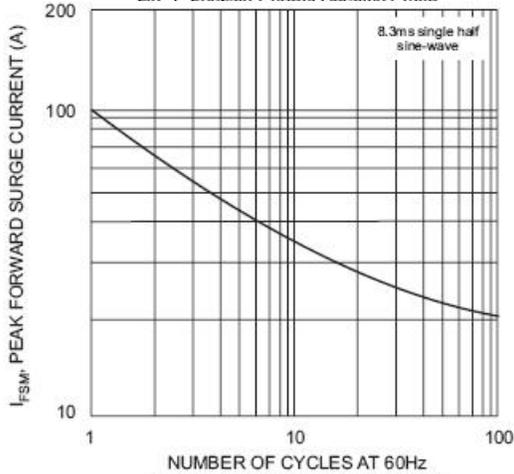


Fig. 3 Peak Forward Surge Current

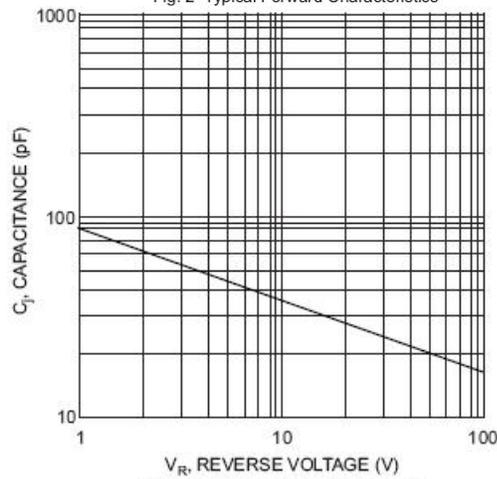
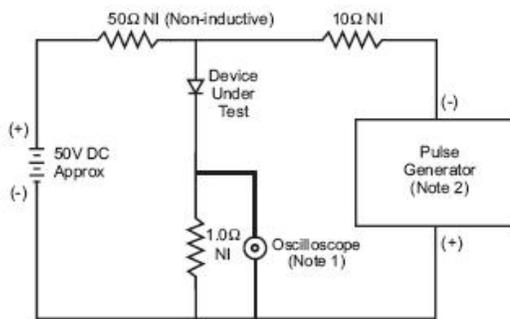


Fig. 4 Typical Junction Capacitance



Notes:
1. Rise Time = 7.0ns max. Input Impedance = 1.0M Ω , 22pF.
2. Rise Time = 10ns max. Input Impedance = 50 Ω .

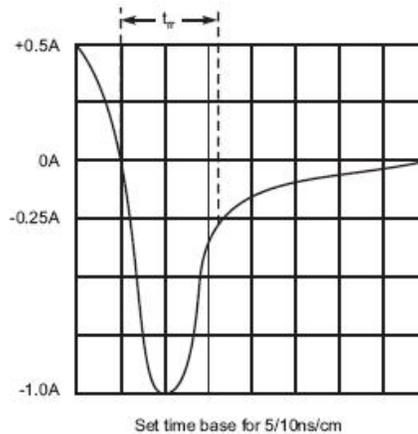


Fig. 5 Reverse Recovery Time Characteristic and Test Circuit

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